IFW

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on the below date:

Date: 3/18/05 Name: Anthony P. Curtis, Ph.D., 46,193 Signature:

BRINKS HOFER GILSON & LIONE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Appln. of:	Shawn D. Rogers et al.
Appln. No.:	10/803,311
Filed:	March 18, 2004
For:	Circuit and Method for Broadband Switching Noise Suppression in Multilayer Printed Circuit Boards Using Localized Lattice Structures
Attorney Docket No:	10599/131

Examiner: Not yet assigned

Art Unit: 2841

Mail Stop Amendment
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL

Sir:

Attached is/are:

☒ Transmittal Cover Letter (1p. Filed in Dup.); Information Disclosure Statement (3pp.); PTO Form 1449 (4p.); 18 Non-patent cited references

☒ Return Receipt Postcard

Fee calculation:

☒ No additional fee is required.

☐ Small Entity.

☐ An extension fee in an amount of $_____ for a _____-month extension of time under 37 C.F.R. § 1.136(a).

☐ A petition or processing fee in an amount of $_____ under 37 C.F.R. § 1.17(_____).

☐ An additional filing fee has been calculated as shown below:

						Small Entity			Not a Small Entity	
	Claims Remaining After Amendment		Highest No. Previously Paid For	Present Extra		Rate	Add'l Fee	or	Rate	Add'l Fee
Total		Minus				x $25=			x $50=	
Indep.		Minus				x 100=			x $200=	
First Presentation of Multiple Dep. Claim						+$180=			+ $360=	
						Total	$		Total	$

Fee payment:

☐ A check in the amount of $_____ is enclosed.

☐ Please charge Deposit Account No. 23-1925 in the amount of $. A copy of this Transmittal is enclosed for this purpose.

☐ Payment by credit card in the amount of $_____ (Form PTO-2038 is attached).

☒ The Director is hereby authorized to charge payment of any additional filing fees required under 37 CFR § 1.16 and any patent application processing fees under 37 CFR § 1.17 associated with this paper (including any extension fee required to ensure that this paper is timely filed), or to credit any overpayment, to Deposit Account No. 23-1925.

3/18/05
Date

Respectfully submitted,

Anthony P. Curtis, Ph.D. (Reg. No. 46,193)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Appln. of:	Shawn D. Rogers et al.		
Appln. No.:	10/803,311	Examiner:	Not yet assigned
Filed:	March 18, 2004	Art Unit:	2841
For:	CIRCUIT AND METHOD FOR BROADBAND SWITCHING NOISE SUPPRESSION IN MULTILAYER PRINTED CIRCUIT BOARDS USING LOCALIZED LATTICE STRUCTURES		
Attorney Docket No:	10599/131		

INFORMATION DISCLOSURE STATEMENT

In accordance with the duty of disclosure under 37 C.F.R. §1.56 and §§1.97-1.98, and more particularly in accordance with 37 C.F.R. §1.97(b), Applicants hereby cite the following reference(s):

No.	Date of Publication	Patentee/Applicant/Assignee
5,870,274	February 9, 1999	Lucas
5,079,069	January 7, 1992	Howard et al.
5,010,641	April 30, 1991	Sisler

OTHER ART – NON PATENT LITERATURE DOCUMENTS
Ramesh Abhari and George V. Eleftheriades, "Suppression of the Parallel-Plate Noise in High Speed Circuits Using a Metallic Electromagnetic Band-Gap Structure," 2002 IEEE Microwave Theory and Techniques International Symposium, pp. 493-496.
Telesphor Kamgaing and Omar M. Ramahi, "High-Impedance Electromagnetic Surfaces for Parallel-Plate Mode Suppression in High Speed Digital Systems," IEEE 11th Topical Meeting on Electrical Performance of Electronic Packaging, Oct 21-23, 2002, Monterey, CA, pp. 279-282.
Telesphor Kamgaing and Omar M. Ramahi, " A Novel Power Plane with Integrated Simultaneous Switching Noise Mitigation Capability Using High Impedance Surface," IEEE Microwave and Wireless Components Letters, Vol. 13, No. 1, January 2003, pp. 21-23.
S. Clavijo, R. Diaz, and W. McKinzie, "Design Methodology for Sievenpiper High-Impedance Surfaces: An Artificial Magnetic Conductor for Positive Gain Electrically Small Antennas." Submitted in Oct 2002 to the *IEEE Transactions on Antennas and Propagation* for publication in their Special Issue on Metamaterials. Publication date TBD.
S. Van den Berghe, F. Olyslager, D. De Zutter, J. De Moerloose, and W. Temmerman, "Study of the Ground Bounce Caused by Power Plane Resonances," *IEEE Trans. Electromag. Compat.*, Vol. 40, No. 2, pp. 111-119, May 1998.

N. Na, J. Choi, S. Chun, M. Swaminathan, and J. Srinivasan, "Modeling and Transient Simulation of Planes in Electronic Packages," *IEEE Trans. Advanced Packaging,* Vol. 23, No. 3, pp. 340-352, August 2000.
S. Chun, M. Swaminathan, L. D. Smith, J. Srinivasan Z. Jin and M. K. Iyer, "Modeling of Simultaneous Switching Noise in High Speed Systems," *IEEE Trans. Advanced Packaging,* Vol. 24, No. 2, pp. 132-142, May 2001.
T. Tarvainen, "Simplified Modeling of Parallel Plate Resonances on Multilayer Printed Circuit Boards," *IEEE Trans. Electromag. Compat.,* Vol. 42, No. 3, pp. 284-289, August 2000.
A. R. Djordjevic and T. K. Sarkar, "An Investigation of Delta-I noise on Integrated Circuits," *IEEE Trans. Electromag. Compat.,* Vol. 35, No. 2, pp. 134-147, May 1993. [6] L. D. Smith, "Simultaneous Switch Noise and Power Plane Bounce for CMOS technology," *Proc. IEEE 8th Topical Meeting Elect. Perform. Electron. Packag.*, San Diego, CA, pp. 163-166, October 1999.
L. D. Smith, "Simultaneous Switch Noise and Power Plane Bounce for CMOS technology," *Proc.IEEE 8th Topical Meeting Elect. Perform. Electron. Packag.*, San Diego, CA, pp. 163-166, October 1999.
K. Lee and A. Barber, "Modeling and Analysis of Multichip Module Power Supply planes," *IEEE Trans. Comp., Packaging, Manuf., Tech.-PART B,* Vol. 18, No. 4, pp. 628-638, November 1995.
Edward R. Pillai, "Coax Via—A Technique to Reduce Crosstalk and Enhance Impedance Match at Vias in High-Frequency Multilayer Packages Verified by FDTD and MoM Modeling," *IEEE Trans. Microwave Theory Tech.*, Vol. 45, NO. 10, pp. 1981-1985, October 1997.
H. H. Wu, J. W. Meyer, K. Lee and A. Barber "Accurate Power Supply and Ground Plane Pair Models," *IEEE Trans. Advanced Packaging,* Vol. 22, No. 3, pp. 259-266, August 1999.
W. Pinello, A. C. Cangellaris and A. Ruehli, "Hybrid Electromagnetic Modeling of Noise Interactions in Packaged Electronics Based on the Partial-Element Equivalent Circuit Formulation," *IEEE Trans. Microwave Theory Tech.,* Vol. 45, No. 10, pp. 1889-1896, October 1997.
B. Archambeault and A. E. Ruehli, "Analysis of Power/Ground-plane EMI Decoupling Performance Using the Partial-Element Equivalent Circuit Technique," *IEEE Trans. Electromag. Compat.,* Vol. 43, No. 4, pp. 437-445, November 2001. Page 18 of 15119
M. Piket-May, A.Taflove and J. Baron, "FD-TD Modeling of Digital Signal Propagation in 3-D Circuits with Passive and Active Loads," *IEEE Trans. Microwave Theory Tech.,* Vol. 42, No. 8, pps. 1514-1523, August 1994.
R. Mittra, W. D. Becker and P. H. Harms, "A General Purpose Maxwell Solver for the Extraction of Equivalent Circuits of Electronic Package Components for Circuit Simulation," *IEEE Trans. Circuits and Systems-Part 1: Fundamental Theory and Applications,* Vol. 39, No. 11, pp. 964-973, November 1992.
T. H. Hubing, J. L. Drewniak, T. P. Van Doren and D. M. Hockason, "Power Bus Decoupling on Multilayer Printed Circuit Boards" *IEEE Trans. Electromag. Compat.,* Vol. 37, No. 2, pp. 155-166, May 1995.

Applicants are enclosing Form PTO-1449 (three sheets), along with a copy of each listed reference for which a copy is required under 37 C.F.R. §1.98(a)(2). As each of the listed references is in English, no further commentary is believed to be necessary,

37 C.F.R §1.98(a)(3). Applicants respectfully request the Examiner's consideration of the above reference(s) and entry thereof into the record of this application.

By submitting this Statement, Applicants are attempting to fully comply with the duty of candor and good faith mandated by 37 C.F.R. §1.56. As such, this Statement is not intended to constitute an admission that any of the enclosed references, or other information referred to therein, constitutes "prior art" or is otherwise "material to patentability," as that phrase is defined in 37 C.F.R. §1.56(a).

Applicants have calculated no fee to be due in connection with the filing of this Statement. However, the Director is authorized to charge any fee deficiency associated with the filing of this Statement to a deposit account, as authorized in the Transmittal accompanying this Statement.

Respectfully submitted,

3/18/05
Date

Anthony P. Curtis, Ph.D.
(Reg. No. 46,193)

FORM PTO-1449	SERIAL NO. 10/803,311	CASE NO. 10599/131
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	FILING DATE March 18, 2004	GROUP ART UNIT 2841
(use several sheets if necessary)	APPLICANT(S): Shawn D. Rogers et al.	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER Number-Kind Code (if known)	DATE	NAME	CLASS/ SUBCLASS	FILING DATE
	A1	5,870,274	February 9, 1999	Lucas		
	A2	5,079,069	January 7, 1992	Howard et al.		
	A3	5,010,641	April 30, 1991	Sisler		

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER Number-Kind Code (if known)	DATE	COUNTRY	CLASS/ SUBCLASS	TRANSLATION YES OR NO

EXAMINER INITIAL		OTHER ART – NON PATENT LITERATURE DOCUMENTS (Include name of author, title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date page(s), volume-issue number(s), publisher, city and/or country where published.
	A4	Ramesh Abhari and George V. Eleftheriades, "Suppression of the Parallel-Plate Noise in High Speed Circuits Using a Metallic Electromagnetic Band-Gap Structure," 2002 IEEE Microwave Theory and Techniques International Symposium, pp. 493-496.
	A5	Telesphor Kamgaing and Omar M. Ramahi, "High-Impedance Electromagnetic Surfaces for Parallel-Plate Mode Suppression in High Speed Digital Systems," IEEE 11th Topical Meeting on Electrical Performance of Electronic Packaging, Oct 21-23, 2002, Monterey, CA, pp. 279-282.
	A6	Telesphor Kamgaing and Omar M. Ramahi, " A Novel Power Plane with Integrated Simultaneous Switching Noise Mitigation Capability Using High Impedance Surface," IEEE Microwave and Wireless Components Letters, Vol. 13, No. 1, January 2003, pp. 21-23.
	A7	S. Clavijo, R. Diaz, and W. McKinzie, "Design Methodology for Sievenpiper High-Impedance Surfaces: An Artificial Magnetic Conductor for Positive Gain Electrically Small Antennas." Submitted in Oct 2002 to the *IEEE Transactions on Antennas and Propagation* for publication in their Special Issue on Metamaterials. Publication date TBD.
	A8	S. Van den Berghe, F. Olyslager, D. De Zutter, J. De Moerloose, and W. Temmerman, "Study of the Ground Bounce Caused by Power Plane Resonances," *IEEE Trans. Electromag. Compat.*, Vol. 40, No. 2, pp. 111-119, May 1998.
	A9	N. Na, J. Choi, S. Chun, M. Swaminathan, and J. Srinivasan, "Modeling and Transient Simulation of Planes in Electronic Packages," *IEEE Trans. Advanced Packaging,* Vol. 23, No. 3, pp. 340-352, August 2000.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449	SERIAL NO. 10/803,311	CASE NO. 10599/131
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	FILING DATE March 18, 2004	GROUP ART UNIT 2841
(use several sheets if necessary)	APPLICANT(S): Shawn D. Rogers et al.	

EXAMINER INITIAL	OTHER ART – NON PATENT LITERATURE DOCUMENTS (Include name of author, title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date page(s), volume-issue number(s), publisher, city and/or country where published.	
	A10	S. Chun, M. Swaminathan, L. D. Smith, J. Srinivasan Z. Jin and M. K. Iyer, "Modeling of Simultaneous Switching Noise in High Speed Systems," *IEEE Trans. Advanced Packaging,* Vol. 24, No. 2, pp. 132-142, May 2001.
	A11	T. Tarvainen, "Simplified Modeling of Parallel Plate Resonances on Multilayer Printed Circuit Boards," *IEEE Trans. Electromag. Compat.,* Vol. 42, No. 3, pp. 284-289, August 2000.
	A12	A. R. Djordjevic and T. K. Sarkar, "An Investigation of Delta-I noise on Integrated Circuits," *IEEE Trans. Electromag. Compat.,* Vol. 35, No. 2, pp. 134-147, May 1993. [6] L. D. Smith, "Simultaneous Switch Noise and Power Plane Bounce for CMOS technology," *Proc. IEEE 8th Topical Meeting Elect. Perform. Electron. Packag.*, San Diego, CA, pp. 163-166, October 1999.
	A13	L. D. Smith, "Simultaneous Switch Noise and Power Plane Bounce for CMOS technology," *Proc.IEEE 8th Topical Meeting Elect. Perform. Electron. Packag.*, San Diego, CA, pp. 163-166, October 1999.
	A14	K. Lee and A. Barber, "Modeling and Analysis of Multichip Module Power Supply planes;" *IEEE Trans. Comp., Packaging, Manuf., Tech.-PART B,* Vol. 18, No. 4, pp. 628-638, November 1995.
	A15	Edward R. Pillai, "Coax Via—A Technique to Reduce Crosstalk and Enhance Impedance Match at Vias in High-Frequency Multilayer Packages Verified by FDTD and MoM Modeling," *IEEE Trans. Microwave Theory Tech.*, Vol. 45, NO. 10, pp. 1981-1985, October 1997.
	A16	H. H. Wu, J. W. Meyer, K. Lee and A. Barber "Accurate Power Supply and Ground Plane Pair Models," *IEEE Trans. Advanced Packaging,* Vol. 22, No. 3, pp. 259-266, August 1999.
	A17	W. Pinello, A. C. Cangellaris and A. Ruehli, "Hybrid Electromagnetic Modeling of Noise Interactions in Packaged Electronics Based on the Partial-Element Equivalent Circuit Formulation," *IEEE Trans. Microwave Theory Tech.,* Vol. 45, No. 10, pp. 1889-1896, October 1997.
	A18	B. Archambeault and A. E. Ruehli, "Analysis of Power/Ground-plane EMI Decoupling Performance Using the Partial-Element Equivalent Circuit Technique," *IEEE Trans. Electromag. Compat.,* Vol. 43, No. 4, pp. 437-445, November 2001. Page 18 of 15119
	A19	M. Piket-May, A.Taflove and J. Baron, "FD-TD Modeling of Digital Signal Propagation in 3-D Circuits with Passive and Active Loads," *IEEE Trans. Microwave Theory Tech.,* Vol. 42, No. 8, pps. 1514-1523, August 1994.
	A20	R. Mittra, W. D. Becker and P. H. Harms, "A General Purpose Maxwell Solver for the Extraction of Equivalent Circuits of Electronic Package Components for Circuit Simulation," *IEEE Trans. Circuits and Systems-Part 1: Fundamental Theory and Applications,* Vol. 39, No. 11, pp. 964-973, November 1992.
	A21	T. H. Hubing, J. L. Drewniak, T. P. Van Doren and D. M. Hockason, "Power Bus Decoupling on Multilayer Printed Circuit Boards" *IEEE Trans. Electromag. Compat.,* Vol. 37, No. 2, pp. 155-166, May 1995.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.